Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A method of fabricating a non-volatile memory, comprising the steps of:
providing a substrate;
forming a longitudinal strip of stacked layer over the substrate, wherein the longitudinal strip is a stack that includes a gate dielectric layer, a conductive layer and a cap layer;
forming a buried bit line in the substrate on each side of the longitudinal strip;
patterning the longitudinal strip to form a plurality of stacked blocks;
forming a dielectric layer over the substrate, wherein the dielectric layer exposes the cap layers of the stacked blocks;
removing the cap layers of some of the stacked blocks so that a portion of the conductive layer of the stacked blocks is exposed; and
forming a word line over the dielectric layer to connect stacked blocks in the same row serially.

[c2] 2. The method of claim 1, wherein the cap layer has an etching rate greater than the dielectric layer.

[c3] 3. The method of claim 1, wherein material constituting the cap layer includes silicon oxide.

[c4] 4. The method of claim 1, wherein material constituting the dielectric layer includes silicon nitride.

[c5] 5. The method of claim 1, wherein material constituting the word line includes metallic substance or polysilicon.

[c6] 6. The method of claim 1, wherein material constituting the conductive material includes polysilicon.

[c7] 7. The method of claim 1, wherein the step of forming the buried bit line includes conducting an ion implantation using the longitudinal strip as an implant mask.

[c8] 8. The method of claim 1, wherein the step of removing the cap layers of some stacked blocks includes the substeps of:
forming a code-masking layer over the dielectric layer to expose the cap layers of some stacked blocks; and
conducting an anisotropic etching process to remove the cap layers.

[c9] 9. The method of claim 8, wherein the anisotropic etching includes a wet etching process or a dry etching process.